CLAIMS

1. A method for testing an integrated circuit using dual scan chains, comprising:

scanning a first test data from an input pin into a first scan chain during a first state of a clock cycle; and

scanning a second test data from the input pin into a second scan chain during a second state of the clock cycle.

2. The method of claim 1 further comprising:

receiving test data from the first scan chain at an output pin during the first state of the clock cycle.

3. The method of claim 2 further comprising:

receiving test data from the second scan chain at the output pin during the second state of the clock cycle.

4. The method of claim 3 further comprising:

sending test data from the first and second scan chains to a multiplexor;

applying a select signal to the multiplexor based on the state of the clock signal; and

causing the multiplexor to output test data from either the first or second scan chain to the output pin based on the select signal.

5. The method of claim 1, wherein scanning the first test data comprises:

using a return-to-one clock waveform; and

using positive, negative, or mixed edge triggered scan flip-flops in the first scan chain;

wherein scanning the second test data comprises;

using the return-to-one clock waveform; and

using positive, negative, or mixed edge triggered scan flip-flops in the second scan chain.

6. The method of claim 5, further comprising:

associating a lockup register with a beginning flip-flop or an ending flip-flop of the first or second scan chains based on return-to-one selection criteria.

7. The method of claim 6, wherein associating a lockup register with the beginning flip-flop or the ending flip-flop of the first or second scan chains based on return-to-one selection criteria comprises:

associating a negative edge triggered scan-in lockup register with the beginning flip-flop of the first scan chain if the beginning flip-flop of the first scan chain has a positive edge trigger;

associating a positive edge triggered scan-in lockup register with the beginning flip-flop of the second scan chain if the beginning flip-flop of the second scan chain has a negative edge trigger; and

associating a negative edge triggered scan-out lockup register if the ending flip-flop of the second scan chain has a negative edge trigger.

8. The method of claim 1, wherein scanning the first test data comprises:

using a return-to-zero clock waveform; and

using positive, negative, or mixed edge triggered scan flip-flops in the first scan chain;

wherein scanning the second test data comprises;

using the return-to-zero clock waveform; and

using positive, negative, or mixed edge triggered scan flip-flops in the second scan chain.

9. The method of claim 8, further comprising:

associating a lockup register with a beginning flip-flop or an ending flip-flop of the first or second scan chains based on return-to-zero selection criteria.

10. The method of claim 9, wherein associating a lockup register with the beginning flip-flop or the ending flip-flop of the first or second scan chains based on return-to-zero selection criteria comprises:

associating a positive edge triggered scan-in lockup register with the beginning flip-flop of the first scan chain if the beginning flip-flop of the first scan chain has a negative edge trigger;

associating a negative edge triggered scan-in lockup register with the beginning flip-flop of the second scan chain if the beginning flip-flop of the second scan chain has a positive edge trigger; and

associating a positive edge triggered scan-out lockup register if the ending flip-flop of the second scan chain has a positive edge trigger.

11. An apparatus for testing an integrated circuit using dual scan chains, comprising:

means for scanning a first test data from an input pin into a first scan chain during a first state of a clock cycle; and

means for scanning a second test data from the input pin into a second scan chain during a second state of the clock cycle.

12. The apparatus of claim 11 further comprising:

means for receiving test data from the first scan chain at an output pin during the first state of the clock cycle.

13. The apparatus of claim 12 further comprising:

means for receiving test data from the second scan chain at the output pin during the second state of the clock cycle.

14. The apparatus of claim 13 further comprising:

means for sending test data from the first and second scan chains to a multiplexor;

means for applying a select signal to the multiplexor based on the state of the clock signal; and

means for causing the multiplexor to output test data from either the first or second scan chain to the output pin based on the select signal.

15. The apparatus of claim 11, wherein said means for scanning the first test data comprises:

means for using a return-to-one clock waveform; and

means for using positive, negative, or mixed edge triggered scan flip-flops in the first scan chain;

wherein said means for scanning the second test data comprises;

means for using the return-to-one clock waveform; and

means for using positive, negative, or mixed edge triggered scan flip-flops in the second scan chain.

16. The apparatus of claim 15, further comprising:

means for associating a lockup register with a beginning flip-flop or an ending flip-flop of the first or second scan chains based on return-to-one selection criteria.

17. The apparatus of claim 16, wherein said means for associating a lockup register with the beginning flip-flop or the ending flip-flop of the first or second scan chains based on return-to-one selection criteria comprises:

means for associating a negative edge triggered scan-in lockup register with the beginning flip-flop of the first scan chain if the beginning flip-flop of the first scan chain has a positive edge trigger;

means for associating a positive edge triggered scan-in lockup register with the beginning flip-flop of the second scan chain if the beginning flip-flop of the second scan chain has a negative edge trigger; and

means for associating a negative edge triggered scan-out lockup register if the ending flip-flop of the second scan chain has a negative edge trigger.

18. The apparatus of claim 11, wherein said means for scanning the first test data comprises:

means for using a return-to-zero clock waveform; and

means for using positive, negative, or mixed edge triggered scan flip-flops in the first scan chain;

wherein said means for scanning the second test data comprises;

means for using the return-to-zero clock waveform; and

means for using positive, negative, or mixed edge triggered scan flip-flops in the second scan chain.

19. The apparatus of claim 18, further comprising:

means for associating a lockup register with a beginning flip-flop or an ending flip-flop of the first or second scan chains based on return-to-zero selection criteria.

20. The apparatus of claim 19, wherein said means for associating a lockup register with the beginning flip-flop or the ending flip-flop of the first or second scan chains based on return-to-zero selection criteria comprises:

means for associating a positive edge triggered scan-in lockup register with the beginning flip-flop of the first scan chain if the beginning flip-flop of the first scan chain has a negative edge trigger;

means for associating a negative edge triggered scan-in lockup register with the beginning flip-flop of the second scan chain if the beginning flip-flop of the second scan chain has a positive edge trigger; and

means for associating a positive edge triggered scan-out lockup register if the ending flip-flop of the second scan chain has a positive edge trigger.

21. An article of manufacture comprising:

a computer readable medium storing computer instructions, the instructions comprising:

instructions to scan a first test data from an input pin into a first scan chain during a first state of a clock cycle; and

instructions to scan a second test data from the input pin into a second scan chain during a second state of the clock cycle.

22. The article of claim 21, the instructions further comprising:

instructions to receive test data from the first scan chain at an output pin during the first state of the clock cycle.

23. The article of claim 22, the instructions further comprising:

instructions to receive test data from the second scan chain at the output pin during the second state of the clock cycle.